19.3 A WCDMA Transmitter in 0.13µm CMOS Using Direct-Digital RF Modulator

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Component count reduction in multi-standard radio architectures can bring savings in complexity, area, and power consumption if more functions can be integrated into a smaller number of circuit blocks. The WCDMA system sets challenging requirements for the transmitter: more than 70dB of power control range is required while the transmitter should fulfill the demanding signal linearity specifications. Typically the control range is partitioned between several functional blocks [1], all of which have their effects on the linearity and noise performance of the system. In addition, calibration of the non-idealities in a traditional I/Q-modulator [2] is often necessary which increases complexity.

A WCDMA transmitter based on a direct-digital RF modulator (DDRM) [3] reduces the component count by combining digital-to-analog (D/A) conversion and upconversion into one circuit block. This enables signal conversion from the digital to the analog domain directly in front of the power amplifier (PA) utilizing highly linear but robust mixed-signal design. In addition, a wide power control range can be implemented inside the DDRM with well-controlled signal linearity, LO-leakage, and image-rejection characteristics, eliminating the need for separate variable-gain amplifiers. However, due to the stringent noise floor specifications of cellular systems, higher than 8b resolution used in the previous implementation [3] is required from the converters and the sampling rate needs to be increased in order to lower the quantization noise level. When the DDRM is operating at a higher clock frequency than the digital baseband, the images at the input clock multiples can be partly filtered out in the digital domain. In addition, the use of a high oversampling ratio in the D/A conversion makes it possible to exploit the low-pass filtering effect of the sinc function.

The core of the implemented WCDMA transmitter, shown in Fig. 19.3.1, is the I/Q-modulator, which consists of two 10b digital-to-RF converters (DRFC) operating at a 307.2MHz sampling frequency. The converter, shown in Fig. 19.3.2, is a matrix of conversion cells each of which makes the D/A-conversion and the upconversion for each of the unit digital signals individually. 6 MSBs of the segmented structure are converted by 63 unit cells and the 4 LSBs with 15 cells having their current of $1/16^{th}$ of the MSB current. Thermometer decoders are used for converting the binary input data into the control signals of the conversion cells. Transmitter power control is implemented using a current-steering DAC for generating a variable bias current for the modulator and by scaling the control voltage of the reference circuitry.

The 307.2MHz sample clock of the converters is a 38.4MHz reference clock multiplied by eight, using a delay-locked loop (DLL) due to its potentially lower jitter when compared to more common phase-locked-loop-based (PLL-based) architectures [4]. Also, as the DLL intrinsically synchronizes the input and the output clocks, the transitions in the different clock domains are accurately synchronized. The clock domain conversion of the input data can thus simply be made by using cascaded flip-flops that are synchronized with the different clock signals.

The digital front-end (DFE) provides the image filtering, that is typically implemented with an analog circuit, by attenuating the signal replicas located at the multiples of the input clock frequency. In order to avoid excessive complexity, the filter, which operates at 307.2MHz, is constructed using cascaded IIR and FIR filter elements, as shown in Fig. 19.3.3, where the multipliers are replaced with bit-shifting operations. The FIR blocks generate notches at the most critical frequencies, suppressing images of the input data. The IIR blocks have low-pass responses which filter the images even further. In order to test the functionality of the system with different operational conditions, the implemented digital front-end has a lot of additional programmability in the input and output weighting and in the filter parameters.

Two different measurement setups are used in order to show the modulator performance as a stand-alone chip and to evaluate the whole transmitter performance using a standard commercially available WCDMA PA module with a power gain of 27dB.

Figure 19.3.4 shows the image rejection, LO-leakage, and highest distortion components of the modulator, measured over 90dB of power control range with 3dB steps. The signal is a 1.4MHz full-scale sine wave with 1.9GHz carrier frequency. The result shows that, as the image rejection is mainly determined by the phase mismatch in the LO path, it scales down when the signal power is decreased. Also, the highest distortion component stays below -50dBc over 60dB of control range. This proves that the linearity of the modulator is insensitive to the signal level, despite the low supply voltage of 1.2V. The fine steps inside the 3dB analog steps can be implemented in the digital domain with necessary accuracy.

Figure 19.3.5 shows the WCDMA signal spectrum with the UMTS emission mask at the output of the modulator and at the output of the PA. The measured ACPR performance of the modulator is –58dBc at 5MHz and –61dBc at 10MHz with a WCDMA channel power of –2dBm. The corresponding ACPRs at the output of the PA with +25dBm WCDMA signal power are –41dBc and –56dBc, respectively, showing that the main contributor to the distortion is the PA. The measured noise floor of the modulator at the RX band located at 190MHz offset from the maximum power WCDMA signal is –146dBm/Hz and at the output of the PA is –125dBm/Hz. To avoid blocking the receiver with the transmitter noise, approximately 55dB of attenuation is needed from the duplex filter.

The error-vector-magnitude (EVM) of the WCDMA signal with channel powers from –50dBm to +25dBm at the output of the PA is shown in Fig. 19.3.6. The EVM stays below 2% over 60dB of control range with extensive margin to the system specification of 17.5%. Even at the lowest signal level where the LO leakage is limiting the performance, the EVM is less than 10%.

The analog power consumption of the whole modulator chip with –2dBm WCDMA output signal is 92mW, which scales down to 46mW with –45dBm signal level. The digital parts consume 65mW which can be dramatically reduced by removing the controllability from the DFE that is implemented for prototype testing purposes. The micrograph of the implemented chip is shown in Fig. 19.3.7. The total silicon area is 2.1×1.9µm. The chip is fabricated in a standard digital 1P6M 0.13µm 1.2V CMOS process.

Acknowledgements:
The authors would like to thank Julius Koskela, Panu Siukonen and Paavo Kosonen for their contributions.

References:
[1] V. Leung, L. Larson, and P. Gudem, "Digital-IF WCDMA Handset Transmitter IC in 0.25µm SiGe BiCMOS," *ISSCC Dig. Tech. Papers*, pp182-183, Feb., 2004.
[2] G. Brenna, D. Tschopp, and Q. Huang, "Carrier Leakage Suppression in Direct-Conversion WCDMA Transmitter," *ISSCC Dig. Tech. Papers*, pp 270-271, Feb., 2003.
[3] P. Eloranta and P. Seppinen, "Direct-Digital RF Modulator IC in 0.13µm CMOS for Wide-Band Multi-Radio Applications," *ISSCC Dig. Tech. Papers*, pp. 532-533, Feb., 2005.
[4] L. Rui and D.M. Santos, "Oscillatorless Clock Multiplication," *Proc. IEEE ISCAS*, vol. 4, pp. 630-633, May, 2001.

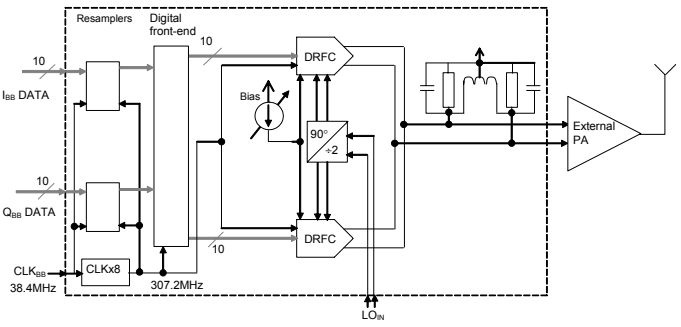

Figure 19.3.1: Block diagram of the WCDMA transmitter.

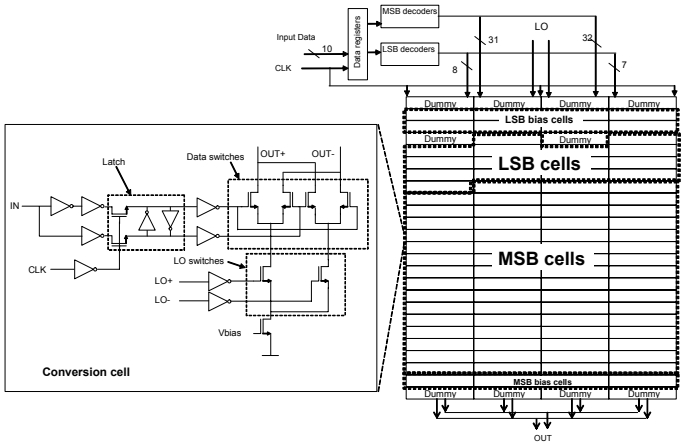

Figure 19.3.2: Converter architecture.

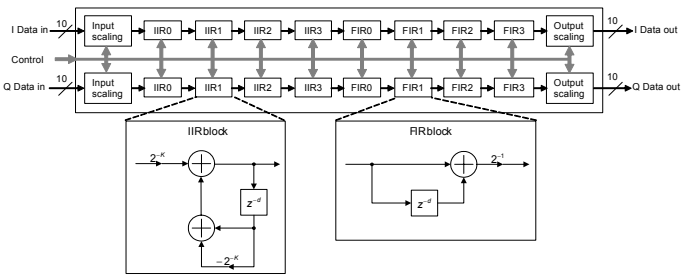

Figure 19.3.3: Block diagram of the digital front-end.

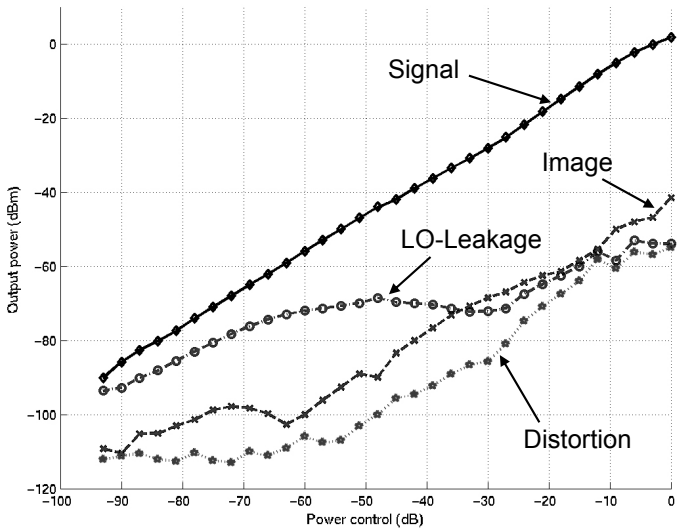

Figure 19.3.4: LO-leakage, image-rejection, and distortion performance of the modulator.

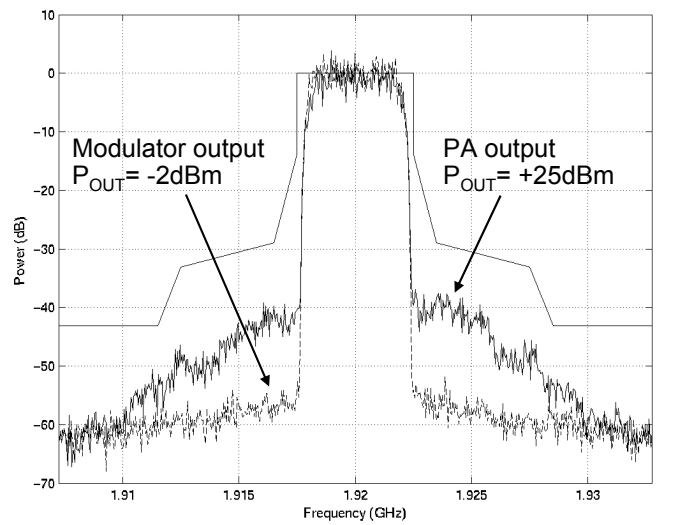

Figure 19.3.5: WCDMA spectrum versus UMTS emission mask.

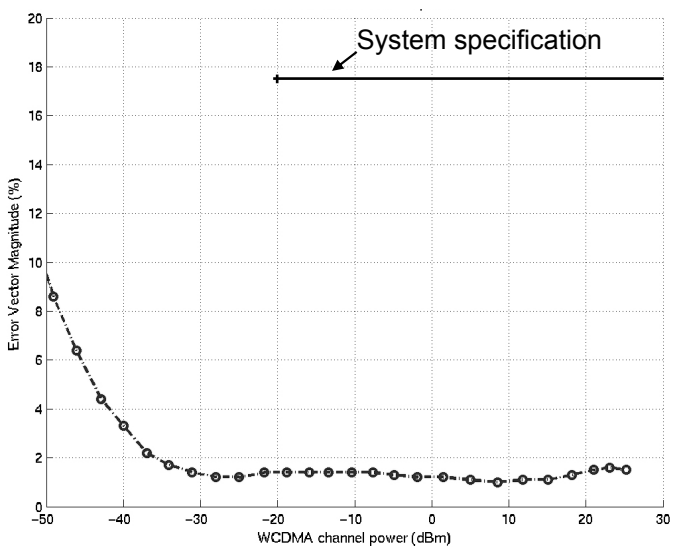

Figure 19.3.6: WCDMA EVM versus channel power.

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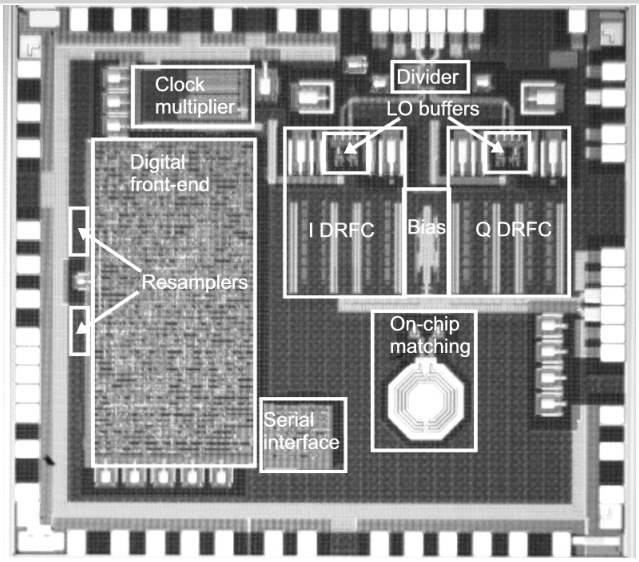

Figure 19.3.7: Chip micrograph.

